Addendum No. 5 to RFP No. 0011204
February 21st, 2004

Except as specifically modified herein, this RFP remains unchanged. Proposers are reminded that receipt of this Addendum No.5 must be acknowledged on Attachment A-1 or A-5 to the solicitation.

Clarification: The NVMM specimen contract states that Phase 1 can consist of either elements or a subassembly. JPL would welcome proposals which envisioned the design and manufacture of suitable elements in Phase 1 and a subassembly design based upon those elements for Phase 2

The following questions and answers are in regards to JPL D-27606; "Non-Volatile Mass memory Functional requirements":

Question 1: In paragraph 10, Subassembly dimension and subassembly mass: Are the dimension .03m3 and mass of 31kg based upon the 640Gbit mass memory system; diagram shown in figure 1, page 10?

Response 1: Figure 1 refers to the block diagram for a non-volatile memory subassembly. The bracketed dimensions and mass allocations are also for a subassembly.

Question 2: Since this is a non-volatile SSR it would seem that the bulk of the memory would be on for a limited amount of time over the 20-year mission life. Is there or may we propose a power profile, which keeps only a small portion of the unit powered on all the time with the remaining memory powered on for a limited amount of time (radiation tolerant and radiation soft devices)? Or does JPL plan to have full 640 Gbit memory per the radiation requirements defined in the paragraph 8.3?

Also in regards to the 1.5E13 write cycle requirement, can this requirement be applied to a smaller portion of the memory with the bulk of the memory seeing a reduced requirement?

Response 2: No power or usage profile exists at this time.

Question 3: In regard to Figure 1, can it be assumed that the Memory Controller is the PCI Master? If so, will drivers need to be written to run on the Memory Controller and control the 7 PCI cards? If so, is there a general processing requirement or RTOS requirement? If the Memory Controller is a slave then should we assume the need for a driver to run on one of the PCI slots?

Response 3: The inclusion of PCI slots as the means for the spacecraft system to interface with the mass memory subassembly was selected as a means to expedite design and development of the mass memory subassembly. The processing requirement is stated in §6.3.3 of the functional requirements document. Selection of an appropriate operating system (if any) for the purposes of controlling the mass memory subassembly is up to proposer. The PCI slots provide a well-defined means of interfacing the mass memory subassembly to the spacecraft system. Any controller internal to the mass memory subassembly would not be an occupant of the 7 slots.

Question 4: Is the density and size of 25 functionally tested NVMM elements consistent with the mass, weight and size of 640Gbit or it could be any size?

Response 4: There are two possible answers to this question: if a subassembly is proposed then it shall be based upon a design of elements that satisfy the various requirements specified in the supporting documents (FR, applicable docs, mission assurance, parts quality, etc.) designed as to permit a subassembly of appropriate size. On the other hand, if elements are proposed then they shall be of such design, quality, and capacity as to permit the design, manufacture, and test of a subassembly that would meet the constraints specified.